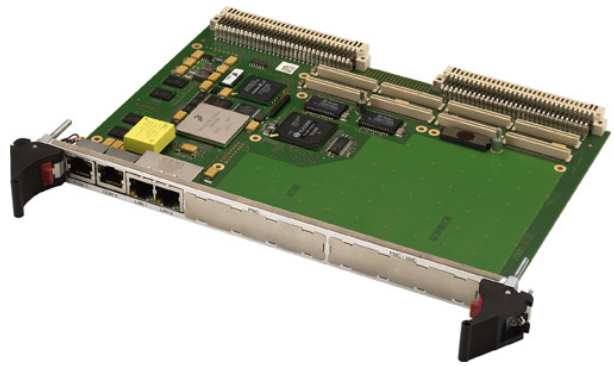
Embedded Solutions

A17 - 6U MPC8548 VMEbus 2eSST CPU Board



- **PowerPC® MPC8548 (or MPC8543), up to 1.5 GHz**
- **1-slot 2eSST VMEbus master and slave**
- **Up to 2 GB (ECC) DDR2 RAM**
- **Flash Disk, FRAM**
- **2 Gb Ethernet, 2 COMs at front**
- **2 Gb Ethernet via P0**
- **2 PMC slots (1 slot also XMC)**
- **FPGA for individual I/O functions**
- **MENMON™ BIOS for PowerPC® cards**
- **-40 to +85°C screened**

The A17 is an advanced PowerPC® based single-board computer for embedded applications and can act as a master or a slave in a legacy VMEbus environment. Using the TSI148 bridge controller the CPU card provides 2eSST performance levels while maintaining backwards compatibility with older standards such as VME64 and VME32. The 2eSST protocol is based on synchronous data transfer and thus doubles the theoretical VME transaction bandwidth to transfer rates of up to 320 MB/s.
The A17 is controlled by an MPC8548, or optionally an MPC8543 PowerPC® processor (alternatively with encryption unit) with clock frequencies between 800 MHz and 1.5 GHz. The SBC is equipped with ECC-controlled DDR2 RAM for data storage, with a Flash disk for program storage as well as with non-volatile FRAM. The board provides front-panel access for two Gigabit Ethernet and two COM interfaces via four RJ45 connectors. Another two Gigabit Ethernet channels are available at the optional P0 rear connector to support Ethernet on the backplane complying with ANSI/VITA 31.1-2003.
The two PMC slots on the A17 support PMC modules working with 32-bit/33-MHz up to 64-bit/66-MHz. One of the mezzanine slots supports rear I/O and can also be used for XMC modules with a PCI Express® x1, x2, or x4 link. The second (PMC only) slot is connected to the onboard FPGA and can thus act as the physical layer for additional functions implemented in the FPGA. The PMC/XMC slots allow flexible extension to the A17, adding functions such as graphics, mass storage, further Ethernet, or a simple FPGA-backed physical layer.
Even more I/O functions such as graphics, touch, CAN, binary I/O etc. can be realized as IP cores in FPGA for the needs of the individual application.
The A17 comes with MENMON™ support. This firmware/BIOS can be used for bootstrapping operating systems (from disk, Flash or network), for hardware testing, or for debugging applications without running any operating system.

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Technical Data

CPU
- PowerPC® PowerQUICC™ III MPC8548, MPC8548E, MPC8543 or MPC8543E
  - 800 MHz up to 1.5 GHz
  - Please see Standard Configurations for available standard versions.
  - e500 PowerPC® core with MMU and double-precision embedded scalar and vector floating-point APU
  - Integrated Northbridge and Southbridge

Memory
- 2x32 KB L1 data and instruction cache, 512 KB/256 KB L2 cache integrated in MPC8548/MPC8543
- Up to 2 GB SDRAM system memory
  - Soldered
  - DDR2 with or without ECC
  - Up to 300 MHz memory bus frequency, depending on CPU
- Up to 4 GB soldered Flash disk (SSD solid state disk)
  - Higher capacity possible if components are available
  - FPGA-controlled
- 16 MB boot Flash
- 128 KB non-volatile FRAM
- Serial EEPROM 8 kbits for factory settings

Mass Storage
- Up to 4 GB soldered ATA Flash disk (SSD solid state disk)
  - Higher capacity possible when components are available
  - FPGA-controlled

I/O
- Ethernet
  - Up to four 10/100/1000Base-T Ethernet channels
  - Two RJ45 connectors at front panel
  - Two front LEDs per channel to signal LAN Link and Activity
  - Two channels accessible via rear I/O on connector P0 complying with ANSI/VITA 31.1-2003 (option)
- Two RS232 UARTs (COM1/2)
  - Two RJ45 connectors at front panel
  - Data rates up to 115.2 kbits/s
  - 16-byte transmit/receive buffer
  - Handshake lines: CTS, RTS
- GPIO
  - 31 GPIO lines
  - FPGA-controlled
  - Connection via PMC1 board-to-board connector J4

Front Connections
- Two Ethernet (RJ45)
- COM1/COM2 (RJ45)
- XMC/PMC 0 and PMC 1

Rear I/O
- Two 10/100/1000Base-T Ethernet on P0 (option)
- Mezzanine rear I/O: PMC 0 on P2

Mezzanine Slots
- Two slots total, one slot usable for PMC or XMC
- One XMC slot
  - Compliant with XMC standard VITA 42.3-2006
  - PCI Express® links: one x1 or one x2 or one x4
- Two PMC slots
  - Compliant with PMC standard IEEE 1386.1
  - Up to 64-bit/64-MHz, 3.3 V V(I/O)
  - PMC I/O module (PIM) support through J4 complying with VITA 35 (PMC 0)

Miscellaneous
- Real-time clock with battery backup
- Temperature sensor, power supervision and watchdog
- Reset button in ejector handle
- One power good LED, three user-configurable LEDs at front

Local PCI Bus
- 64-bit/66-MHz, 3.3 V V(I/O)
- Compliant with PCI Specification 2.2

VMEbus
- TSI148 controller
- Compliant with VME64 Specification
- Supports VME32, VME64, 2eVME and 2eSST (VITA 1.5)
  - Optional single 5V supply for operation in VME32 systems
- Slot-1 function with auto-detection
- Master
  - D08:D16:D32:D64:A16:A24:A32:A64:BLT:MBLT:RMW
- Slave
  - D08:D16:D32:D64:A16:A24:A32:A64:BLT:MBLT
- DMA
- Mailbox functionality
- Bus timer
- Location Monitor
- Interrupter D08(O):I(7-1):ROAK
- Interrupt handler D08(O):IH(7-1)
- Single level 3 fair requester
- Single level 3 arbiter

Electrical Specifications
- Supply voltage/power consumption:
  - +5 V (-3%/+5%), approx. 2.2 A
  - +3.3 V (-3%/+5%), approx. 1.1 A
  - +12 V (-5%/+5%), only provided for PMCs that need 12 V
  - -12 V (-5%/+5%), only provided for PMCs that need 12 V

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Technical Data

Mechanical Specifications
- Dimensions: standard double Eurocard, 233.3 mm x 160 mm
- Weight: 490 g (incl. heat sink, without XMC/PMC modules)

Environmental Specifications
- Temperature range (operation):
  - -40..+85°C (screened)
  - Airflow: min. 10 m³/h
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300 m to +3,000 m
- Shock: 15 g, 11 ms
- Bump: 10 g, 16 ms
- Vibration (sinusoidal): 1 g, 10..150 Hz
- Conformal coating on request

MTBF
- 220,017 h @ 40°C according to IEC/TR 62380 (RDF 2000)

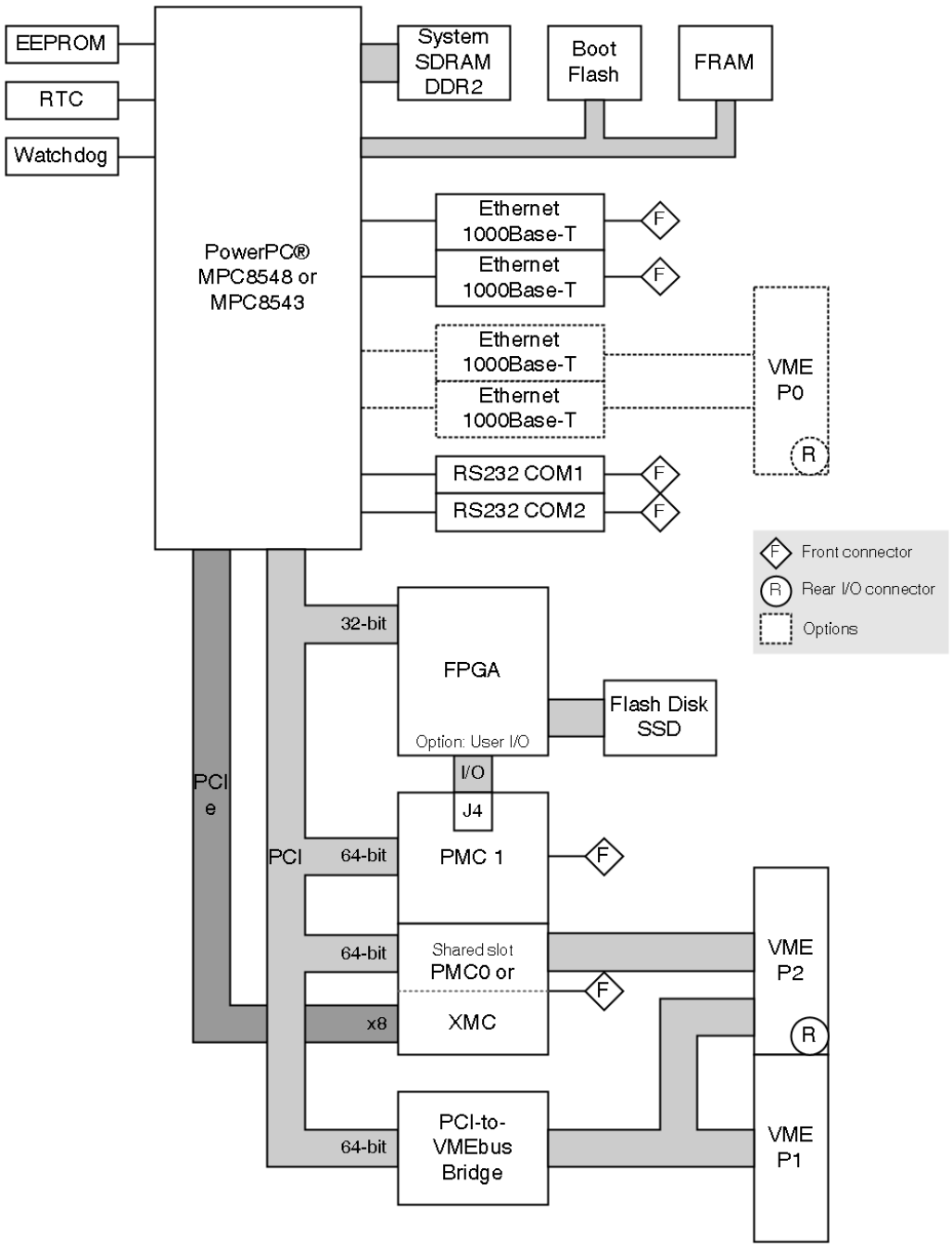
Safety
- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

EMC
- Conforming to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

BIOS
- MENMON™

Software Support
- Linux
- VxWorks®
- QNX® (on request; support of the FPU is currently not provided by QNX®)
- OS-9® (on request)
- For more information on supported operating system versions and drivers see Software.

Diagram


EEPROM
RTC
Watchdog
PowerPC®
MPC8548 or
MPC8543
System
SDRAM
DDR2
Boot
Flash
FRAM
Ethernet
1000Base-T
Ethernet
1000Base-T
Ethernet
1000Base-T
Ethernet
1000Base-T
VME
P0
R
RS232 COM1
RS232 COM2
F
Front connector
R
Rear I/O connector
Options
32-bit
FPGA
Option: User I/O
Flash Disk
SSD
I/O
J4
PCI
e
PCI
64-bit
PMC 1
64-bit
Shared slot
PMC0 or
XMC
x8
VME
P2
R
VME
P1
64-bit
PCI-to-
VMEbus
Bridge

Configuration & Options

Standard Configurations

Article No.	CPU Type	Clock	System RAM	Flash Disk	FRAM	P0 Ethernet	Operation Temperature
01A017-00	MPC8548	1.33 GHz	1 GB ECC	2 GB	128 KB	No	-40..+85°C

Options

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

CPU

- Several PowerQUICC™ III types with different clock frequencies
- MPC8548 or MPC8548E
  - 1 GHz, 1.2 GHz, 1.33 GHz or 1.5 GHz
- MPC8543 or MPC8543E
  - 800 MHz or 1 GHz

Memory

- System RAM
  - 512 MB, 1 GB or 2 GB
  - With or without ECC
- Flash Disk
  - 0 GB up to 4 GB (and more, if components are available)
- FRAM
  - 0 KB or 128 KB

I/O

- Ethernet
  - Two additional Gigabit Ethernet channels on VMEbus P0 rear connector for ANSI/VITA 31.1-2003 support (only with MPC8548)
  - Only two channels (at front) instead of four with MPC8543
- PCI Express® links: one x8 link
  - Reduces operation temperature range because of higher DDR SDRAM clock

FPGA

- The onboard FPGA offers the possibility to add customized I/O functionality.
- FPGA Altera® Cyclone® II EP2C35
  - 33,216 logic elements
  - 483,840 total RAM bits
- Connection
  - Total available pin count: 31 pins
  - Functions available via PMC slot 1 connector Pn4
- You can find more information on our web page "User I/O in FPGA"

VMEbus

- Single 5V supply for operation in VME32 systems

Ordering Information

Standard A17 Models

01A017-00	MPC8548 / 1.33 GHz, 1 GB DDR2 DRAM, 2 GB Flash disk, 128 KB FRAM, P0 not mounted, -40..+85°C screened

Systems & Card Cages

Miscellaneous Accessories

05F006-00	RS232 interface cable RJ45 to 9-pin D-Sub (1 COM to 1 COM), 2m

Software: OS independent

13Z017-06	MDIS5 low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO

Software: Linux

10EM09-91	General Linux BSP for A17, EM9, EM9A, EK9, F50C, F50P and XM50
13Z014-90	Linux device driver (MEN) for PCI-to-VME bridge on A12, A13, A14, A15, A17, A19, A20 and B11

Software: VxWorks

10EM09-60	VxWorks BSP (MEN) for A17, EK9, EM9, EM9A, F50C, F50P and XM50

Software: Firmware/BIOS

14A017-00	MENMON (Firmware) (MEN) for A17 (object code)

Documentation

01A017-DS	A17 Data Sheet
20A017-ER	A17 Errata
20A017-00	A17 User Manual

For the most up-to-date ordering information and direct links to other data sheets and downloads, see the A17 online data sheet under » www.men.de.

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Contact Information

Germany
MEN Mikro Elektronik GmbH
Neuwieder Straße 5-7
90411 Nuremberg
Phone +49-911-99 33 5-0
Fax +49-911-99 33 5-901
E-mail info@men.de
www.men.de

France
MEN Mikro Elektronik SA
18, rue René Cassin
ZA de la Châtelaine
74240 Gaillard
Phone +33 (0) 450-955-312
Fax +33 (0) 450-955-211
E-mail info@men-france.fr
www.men-france.fr

USA
MEN Micro, Inc.
24 North Main Street
Ambler, PA 19002
Phone (215) 542-9575
Fax (215) 542-9577
E-mail sales@menmicro.com
www.menmicro.com

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